浩然电子 Hasion Electronics

HS-NM5300

Datasheet

English Ver. 1.0

2008-6

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Introduction:

HS-W5300 is a network module that integrated W5300 (TCP/IP + Ethernet MAC + Ethernet PHY), RJ-45 and other components. HS-NM5300 can be configured to work in multi operation mode, such as 8/16 data bus, internal PHY/external PHY, internal PHY operation mode etc. it provides an ideal option to carry out embedded network rapidly for engineers.

Fig.1 HS-NM5300A Picture

Features:

- Supports hardwired TCP/IP protocols : TCP,UDP, ICMP, IPv4, ARP, IGMPv2, PPPoE, Ethernet. Supports hybrid TCP/IP stack(software and hardware TCP/IP stack);
- Supports 8 independent SOCKETs simultaneously;
- High network performance : Up to 50Mbps;
- Supports PPPoE connection (with PAP/CHAP Authentication mode);
- Internal 128Kbytes memory for data communication (Internal TX/RX memory). More flexible allocation internal TX/RX memory according to application throughput. Supports memory-to-memory DMA (only 16bit Data bus width & slave mode);
- Embedded 10BaseT/100BaseTX Ethernet PHY. Supports auto negotiation (Full-duplex and half duplex). Supports auto MDI/MDIX(Crossover). Supports a external PHY instead of the internal PHY;
- Select 16/8 bit data bus width through jumper
- Supports 2 host interface mode(Direct address mode & Indirect address mode)
- 3.3V operation with 5V I/O signal tolerance;
- Interfaces with Two 2.0mm pitch 2 * 16 header pin;
- The module PCB dimension: 50mm*28mm

Please refer to the W5300 Datasheet when use HS-NM5300A module.

Pin Assignments:

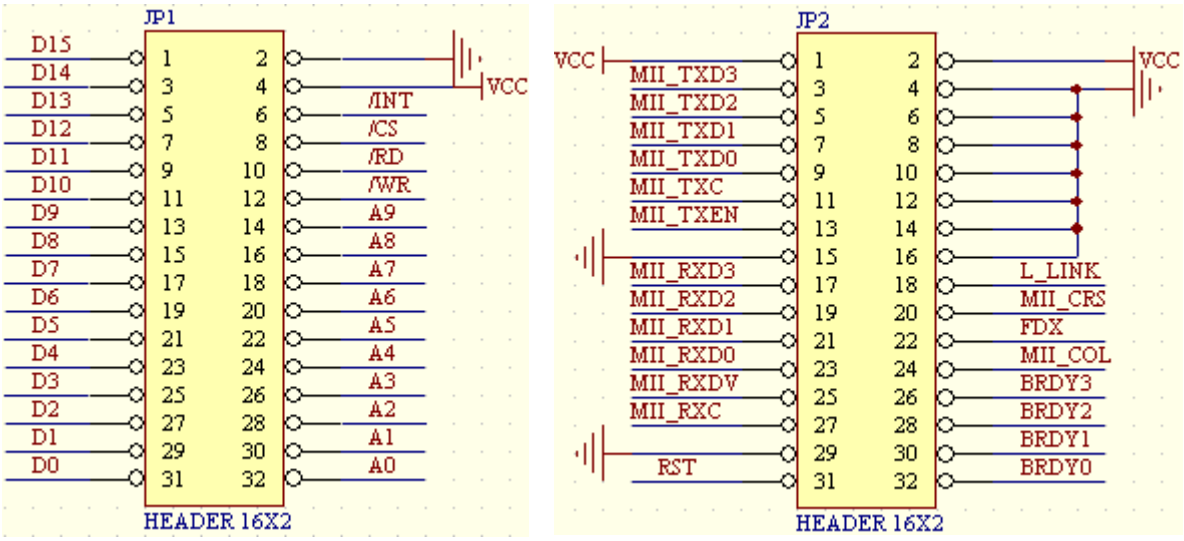

图 2 HS-NM5300A 排针引线图

JP1 Definition:

Pin Number	Definition	Description
1, 3, 5, 7, 9, 11, 13, 15,	D15~D8	Data D15~D8 These are used for Read/Write operation of W5300 register In case of using 8 bit data bus, they are driven as HIGH-Z
17, 19, 21, 23, 25, 27, 29, 31	D7~D0	Data D7~D0 These are used for Read/Write operation of W5300 register
2	GND	Ground
4	VCC	Power supply: 3.0~3.6V, typical value: 3.3V
6	/INT	Interrupt output, active low
8	/CS	Chip select signal input, active low
10	/RD	Read enable signal input, active low
12	/WR	Write enable signal input, active low
14, 16, 18, 20, 22, 24, 26, 28, 30, 32	A9~A0	Address bus A9~A0

JP2 Definition:

引脚号	定义	说明
1, 2	VCC	Power supply, 3.0~3.6V, typical 3.3V
4, 6, 8, 10, 12, 14, 15, 16, 29	GND	Power Ground
3, 5, 7, 9	RXLED/MII_TXD3 COLLED/MII_TXD2 FDXLED/MII_TXD1 SPDLED/MII_TXD0	At the Internal PHY mode, They are output signals of RXLED, COLLED, FDXLED and SPDLED At the external PHY mode, they are output signals of MII_TXD3 ~ MII_TXD0
11	MII_TXC	At the external PHY mode, it is Transmit Clock Input
13	TXLED/MII_TXEN	At the Internal PHY mode, it is TXLED At the external PHY mode, it is Transmit Enable
17, 19, 21, 23	MII_RXD3 MII_RXD2 MII_RXD1 MII_RXD0	At the external PHY mode, they are input signals of MII_RXD3 ~ MII_RXD0
25	MII_RXDV	At the external PHY mode, it is Receive Data Valid
27	MII_RXC	At the external PHY mode, it is Receive Clock input
18	L_LINK	It indicates the link states of Media (10/100M)
20	MII_CRS	At the external PHY mode, It is signal to notify the link traffic of the media. If carrier of media is not idle (carrier present), it is asserted high.
22	FDX	Full duplex select input at the external PHY mode
24	MII_COL	IP collision detect input at the external PHY mode
26, 28, 30, 32	BRDY3, BRDY2 BRDY1, BRDY0	SOCKET buffer ready indicator

Jumper Configuration:

There are 4 groups of jumper on the back of HS-NM5300A, shown as in Fig3. They are:

1. ROM11 and ROM12
2. ROM01 and ROM02
3. RTM01 and RTM02
4. RB1 and RB2

Fig 3 Jumper on the back of HS-NM5300A

These jumpers are defined as following:

1. The width of Data Bus

RB1	RB2	Description
Shorted	Disconnected	Select 8 bit Data bus
Disconnected	Shorted	Select 16 bit Data Bus

2. Select PHY

RTM01	RTM02	Description
Shorted	Disconnected	Select internal PHY
Disconnected	Shorted	Select external PHY, use crystal clock

3. 内部以太网 PHY 运行选择：

ROM01	ROM02	ROM11	ROM12	Description
Shorted	Disconnected	Shorted	Disconnected	Ethernet auto negotiation
Disconnected	Shorted	Shorted	Disconnected	Ethernet 100Base-TX full duplex auto negotiation
Shorted	Disconnected	Disconnected	Shorted	Ethernet 10Base-T full duplex auto negotiation

外形尺寸

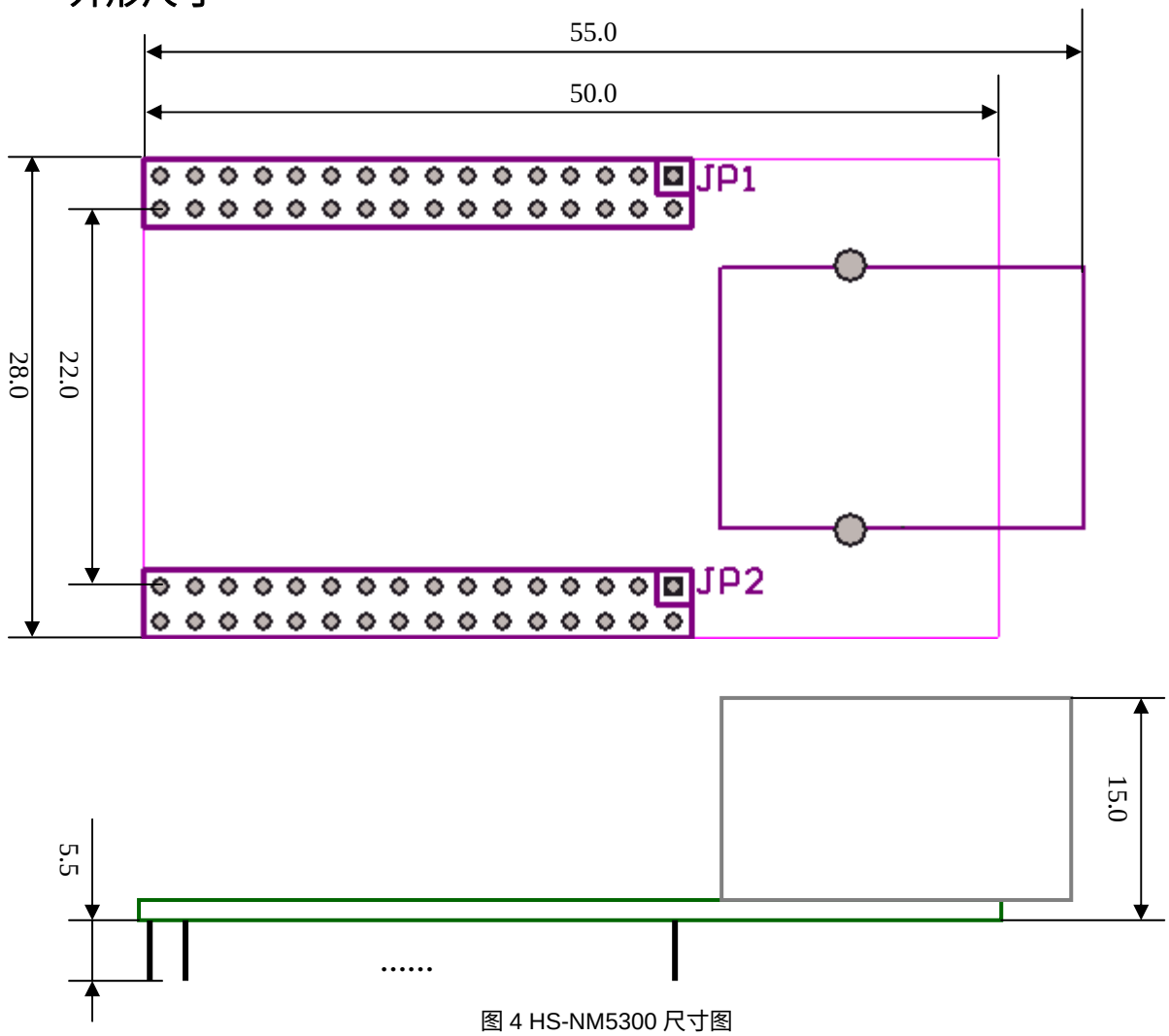

图 4 HS-NM5300 尺寸图

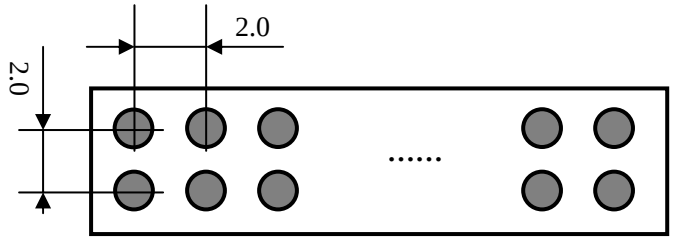

图 5 排针引脚尺寸图